What is claimed is:

1. A return path transmitter for use in conjunction with a local system that generates an analog RF data signal to be conveyed to a head end system, the return path transmitter comprising:

a sample clock generator for generating a sample clock;

an RF signal receiver, coupled to the sample clock generator, for receiving and converting the analog RF data signal into a first data stream of digitized RF data samples at a rate determined by the sample clock;

supplemental channel circuitry for providing a second data stream;

a multiplexor coupled to the RF signal receiver and the supplemental channel circuitry to receive the first data stream and second data stream and to output a combined data stream; and

an optical transmitter for converting the combined data stream into a serialized optical data signal for transmission over an optical fiber.

2. The return path transmitter of claim 1, including:

a first memory device configured to buffer the first data stream;

a second memory device configured to buffer the second data stream;

an output clock generator for generating an output clock having an associated output frequency;

wherein:

the sample clock has an associated sample rate;

the second data stream is generated by the supplemental channel circuitry at a rate that is less than the sample rate;

the multiplexor is configured to monitor a fullness level of the first memory device, output data stored in the first memory device in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and to output data stored in the first memory device and data stored in the second memory device in a second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

3. The return path transmitter of claim 2, wherein:

the supplemental channel circuitry generates maintenance data indicative of an operational state of the return path transmitter.

4. The return path transmitter of claim 2, wherein:

the first memory device comprises a dual ported random access memory device.

5. The return path transmitter of claim 1, including:

a port for receiving a third data stream from a source external to the return path transmitter, the third data stream having a data rate of at least 5 Mb/s; and

merge circuitry for merging the first and third data streams into a merged data stream;

wherein the multiplexor is coupled to the merge circuitry and the supplemental channel circuitry to receive the merged data stream and second data stream and to output the combined data stream.

6. The return path transmitter of claim 5, including:

a first memory for buffering the merged data stream;

a second memory device configured to buffer the second data stream; and

an output clock generator for generating an output clock having an associated output frequency;

wherein:

the sample clock has an associated sample rate frequency;

the second data stream is generated by the supplemental channel circuitry at a rate that is less than the sample rate frequency;

the multiplexor is configured to monitor a fullness level of the first memory device, output data stored in the first memory device in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and to output data stored in the first memory device and data stored in the second memory device in a second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

7. The return path transmitter of claim 5, wherein:

the supplemental channel circuitry generates maintenance data indicative of an operational state of the return path transmitter.

8. The return path transmitter of claim 7, wherein:

the supplemental channel circuitry includes at least one sensor for measuring an operational parameter selected from a group consisting of temperature and supply voltage.

9. The return path transmitter of claim 7, wherein:

the supplemental channel circuitry includes an RF data sampler for sampling data from the first data stream to generate a set of sampled RF data and circuitry for including the sampled RF data in the second data stream.

10. The return path transmitter of claim 1, wherein:

the supplemental channel circuitry generates maintenance data indicative of an operational state of the return path transmitter and includes the maintenance data in the second data stream.

11. The return path transmitter of claim 10, wherein:

the supplemental channel circuitry includes at least one sensor for measuring an operational parameter selected from a group consisting of temperature and supply voltage.

12.. The return path transmitter of claim 10 wherein the supplemental channel circuitry includes an internal memory device configured to store data including at least one of a serial number, model number, date of manufacture, software revision number and hardware revision number of the transmitter, wherein the supplemental channel circuitry is further configured to include at least a portion of the data stored in the internal memory device in the maintenance data.

13. The return path transmitter of claim 1, wherein:

the supplemental channel circuitry includes an RF data sampler for sampling data from the first data stream to generate a set of sampled RF data and circuitry for including the sampled RF data in the second data stream.

14. The return path transmitter of claim 1, wherein:

the supplemental channel circuitry is configured to generate the second data stream intermittently;

the optical transmitter includes circuitry for inserting padding words into the combined data stream so as to maintain the combined data stream at a fixed data rate.

15. A return path transmitter for use in conjunction with first and second local systems that generate first and second respective analog RF data signals to be conveyed to a head end system, the return path transmitter comprising:

a sample clock generator for generating a sample clock;

first and second RF signal receivers, coupled to the sample clock generator, for receiving and converting the first and second respective analog RF data signals into first and second data streams of digitized RF data samples at a rate determined by the sample clock;

supplemental channel circuitry for providing a third data stream;

a multiplexor coupled to the RF signal receivers and the supplemental channel circuitry to receive the first, second and third data streams and to output a combined data stream; and

an optical transmitter for converting the combined data stream into a serialized optical data signal for transmission over an optical fiber.

16. The return path transmitter of claim 15, including:

a first memory device configured to buffer the first data stream;

a second memory device configured to buffer the second data stream;

a third memory device configured to buffer the third data stream;

an output clock generator for generating an output clock having an associated output frequency;

wherein:

the sample clock has an associated sample rate frequency;

the third data stream is generated by the supplemental channel circuitry at a rate that is less than the sample rate frequency;

the multiplexor is configured to monitor a fullness level of the first memory device, output data stored in the first and second memory devices in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and to output data stored in the first and second memory devices and data stored in the third memory device in a

second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

17. The return path transmitter of claim 16, wherein:

the supplemental channel circuitry generates maintenance data indicative of an operational state of the return path transmitter.

18. The return path transmitter of claim 16, wherein:

the first memory device comprises a dual ported random access memory device.

19. A return path transmitter for use in conjunction with first and second local systems that generate first and second respective analog RF data signals to be conveyed to a head end system, the return path transmitter comprising:

a sample clock generator for generating a sample clock;

first and second RF signal receivers, coupled to the sample clock generator, for receiving and converting the first and second respective analog RF data signals into first and second data streams of digitized RF data samples at a rate determined by the sample clock;

a data port for receiving a third data stream from a digital data source external to the return path transmitter, the third data stream having a data rate of at least 5 Mb/s; and

a multiplexor coupled to the RF signal receivers and the data port to receive the first, second and third data streams and to output a combined data stream; and

an optical transmitter for converting the combined data stream into a serialized optical data signal for transmission over an optical fiber.

20. The return path transmitter of claim 19 wherein the digital data source is an Ethernet channel.

21. A return path transmitter for use in conjunction with a local system that generates an analog RF data signal to be conveyed to a head end system, the return path transmitter comprising:

an optical signal receiver configured to receive a digital optical signal and generate therefrom a first digitized RF data stream and a sample clock;

an RF signal receiver, coupled to the optical signal receiver, for receiving and converting the analog RF data signal into a second digitized RF data stream of digitized RF data samples at a rate determined by the sample clock;

a summing circuit for mathematically summing the first and second digitized RF data streams so as to generate a third digitized RF data stream; and

an optical transmitter for converting an output data stream into a serialized optical data signal for transmission over an optical fiber, the output data stream including the third digitized RF data stream.

22. The return path transmitter of claim 21, wherein:

the optical signal receiver is configured to demultiplex data within the received digital optical signal into a first digitized RF data stream and a first non-RF data stream; and

the return path transmitter includes:

a data port for receiving a second non-RF data stream from a digital data source external to the return path transmitter, the second non-RF data stream having a data rate of at least 5 Mb/s;

a full duplex drop and add circuit for extracting a portion of the first non-RF data stream and for replacing the extracted portion of the first non-RF data stream with the second non-RF data stream so as to generate a third non-RF data stream;

a multiplexor coupled to the summing circuit and the full duplex drop and add circuit to receive the third digitized RF data stream and the third non-RF data stream and to output a combined data stream; and

the output data stream converted by the optical transmitter includes the combined data stream.

23. A method transmitting data representing an analog RF signal generated at a local system, comprising:

generating a sample clock having an associated sample rate;

receiving and converting the analog RF signal into a first data stream of digitized RF data samples at the sample rate determined by the sample clock;

providing a second data stream, where second data stream is provided at a rate that is less than the sample rate;

combining the first data stream and second data stream to generate a combined data stream; and

converting the combined data stream into a serialized optical data signal for transmission over an optical fiber.

24. The method of claim 23, including:

generating maintenance data indicative of an operational state of the return path transmitter and including the maintenance data in the second data stream.

25. The method of claim 24, including:

locally storing data including at least one of a serial number, model number, date of manufacture, software revision number and hardware revision number of the transmitter, and including in the second data stream at least a portion of the locally stored data.

26. The method of claim 23, including:

receiving a third data stream from a source external to the return path transmitter, the third data stream having a data rate of at least 5 Mb/s; and

merging the first and third data streams into a merged data stream;

wherein the combining includes combining the merged data stream and second data stream to generate the combined data stream.

27. The method of claim 26, including

buffering the merged data stream in a first memory device;

buffering the second data stream in a second memory device;

generating an output clock having an associated output frequency;

monitoring a fullness level of the first memory device; and

outputting data stored in the first memory device in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and outputting data stored in the first memory device and data stored in the second memory device in a second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

28. The method of claim 23, including

buffering the first data stream in a first memory device;

buffering the second data stream in a second memory device;

generating an output clock having an associated output frequency;

monitoring a fullness level of the first memory device; and

outputting data stored in the first memory device in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and outputting data stored in the first memory device and data stored in the second memory device in a second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

29. The method of claim 23, including:

sampling data from the first data stream to generate a set of sampled RF data and including the sampled RF data in the second data stream.

30. The method of claim 23, wherein:

the second data stream is provided intermittently; and

inserting padding words into the combined data stream so as to maintain the combined data stream at a fixed data rate.

31. A method transmitting data representing first and second analog RF signals generated at first and second local systems, comprising:

generating a sample clock having an associated sample rate;

receiving and converting the first and second respective analog RF data signals into first and second data streams of digitized RF data samples at the sample rate determined by the sample clock;

providing a third data stream;

combining the first, second and third data streams to generate a combined data stream; and

converting the combined data stream into a serialized optical data signal for transmission over an optical fiber.

32. The method of claim 31, including:

buffering the first data stream in a first memory device;

buffering the second data stream in a second memory device;

buffering the third data stream in a third memory device;

generating an output clock having an associated output frequency;

monitoring a fullness level of the first memory device; and

outputting data stored in the first and second memory devices in a first mode when the fullness level of the first memory device is more than a predefined threshold level, and outputting data stored in the first and second memory devices and data stored in the third memory device in a second interleaved mode when the fullness level of the first memory device is less than the predefined threshold level.

33. The method of claim 32, wherein the providing includes receiving the third data stream from a digital data source external to the return path transmitter, the third data stream having a data rate of at least 5 Mb/s.

34. A method transmitting data representing an analog RF signal generated at a local system, comprising:

receive a digital optical signal and generate therefrom a first digitized RF data stream and a sample clock having an associated sample rate;

receiving and converting the analog RF signal into a second digitized RF data stream of digitized RF data samples at a rate determined by the sample clock;

mathematically summing the first and second digitized RF data streams so as to generate a third digitized RF data stream; and

converting an output data stream into a serialized optical data signal for transmission over an optical fiber, the output data stream including the third digitized RF data stream.

35. The method of claim 34, including:

demultiplexing data within the received digital optical signal into a first digitized RF data stream and a first non-RF data stream;

receiving a second non-RF data stream from a digital data source external to the return path transmitter, the second non-RF data stream having a data rate of at least 5 Mb/s;

extracting a portion of the first non-RF data stream and replacing the extracted portion of the first non-RF data stream with the second non-RF data stream so as to generate a third non-RF data stream; and

combining the third digitized RF data stream and the third non-RF data stream and generate a combined data stream;

wherein the output data stream includes the combined data stream.

36. An optical signal receiver comprising:

a signal receiver for receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate;

a memory device configured to store the data stream at a rate corresponding to the first clock rate;

a clock generator for generating a second clock having an associated second clock rate, wherein the clock generator is configured to adjust the second clock rate in accordance with a clock control signal;

logic for reading data from the memory device at a rate corresponding to the second clock rate and for generating a fullness signal that indicates whether the memory device is more full than a predefined threshold fullness level; and

a clock speed adjusting circuit configured to generate the clock control signal in accordance with the fullness signal.

37. The receiver of claim 36, wherein the clock generator includes a voltage controlled crystal oscillator and the clock control signal is a voltage signal.

38. An optical signal receiver comprising:

a signal receiver for receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including a first data stream having an associated first data rate and a second data stream having an associated second data rate that is different from the first data rate; the first data stream comprising a sequence of data frames, each data frame representing a sequence of samples of an RF signal;

a first memory device configured to store the first data stream;

a second memory device configured to store the second data stream;

a demultiplexer for receiving the digital data stream, detecting boundaries of the data frames in the first data stream and storing the data frames in the first memory device,

identifying data in the digital data stream comprising the second data stream and storing the second data stream in the second memory device;

a clock generator for generating a local sample clock having an associated sample clock rate;

logic circuitry for reading data from the first memory device at a rate corresponding to the sample clock rate so as to regenerate the sequence of samples of the RF signal represented by the sequence of data frames comprising the first data stream; and

a digital to analog converter for converting the regenerated sequence of samples at the sample clock rate into an analog signal comprising a regenerated version of the RF signal.

39. The receiver of claim 38, wherein

the logic circuitry is configured to generate a fullness signal that indicates whether the first memory device is more full than a predefined threshold fullness level;

the clock generator is configured to adjust the sample clock rate in accordance with a clock control signal; and

the receiver includes a clock speed adjusting circuit configured to generate the clock control signal in accordance with the fullness signal.

40. The receiver of claim 38, wherein the logic circuitry is configured to read data from the second memory device and transmit the data read from the second memory device to a digital data device.

41. The receiver of claim 40, wherein the digital data device is a data processor.

42. The receiver of claim 40, wherein the digital data device is coupled to a network router for routing data packets in the second data stream.

43. An optical signal receiver comprising:

a signal receiver for receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including first, second and third data streams, the first data stream comprising a first sequence of first data frames, each first data frame representing a sequence of samples of a first RF signal, the second data stream comprising a second sequence of

second data frames, each second data frame representing a sequence of samples of a second RF signal;

a first memory device configured to store the first data stream;

a second memory device configured to store the second data stream;

a third memory device configured to store the third data stream;

a demultiplexer for receiving the digital data stream, detecting boundaries of the first data frames in the first data stream and of the second data frames in the second data stream and storing the first data frames in the first memory device and the second data frames in the second memory device, identifying data in the digital data stream comprising the third data stream and storing the third data stream in the third memory device;

a clock generator for generating a local sample clock having an associated sample clock rate;

logic circuitry for simultaneously reading data from the first and second memory devices at a rate corresponding to the sample clock rate so as to regenerate the sequence of samples of the first RF signal represented by the sequence of first data frames comprising the first data stream and the sequence of samples of the second RF signal represented by the sequence of second data frames comprising the second data stream; and

a first digital to analog converter for converting the regenerated sequence of samples of the first RF signal at the sample clock rate into an analog signal comprising a regenerated version of the first RF signal; and

a second digital to analog converter for converting the regenerated sequence of samples of the second RF signal at the sample clock rate into an analog signal comprising a regenerated version of the second RF signal.

44. The receiver of claim 43, wherein the logic circuitry is configured to read data from the third memory device and transmit the data read from the third memory device to a digital data device.

45. An optical signal receiver comprising:

a signal receiver for receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including a first data stream having an associated first data rate and a second data stream having an associated second data rate that is different from the first data

rate; the first data stream comprising a sequence of data frames, each data frame representing a sequence of summed samples of a plurality of RF signals, each summed sample comprising a mathematical sum of samples of a plurality of distinct RF signals;

a first memory device configured to store the first data stream;

a second memory device configured to store the second data stream;

a demultiplexer for receiving the digital data stream, detecting boundaries of the data frames in the first data stream and storing the data frames in the first memory device, identifying data in the digital data stream comprising the second data stream and storing the second data stream in the second memory device;

a clock generator for generating a local sample clock having an associated sample clock rate;

logic circuitry for reading data from the first memory device at a rate corresponding to the sample clock rate so as to regenerate the sequence of summed samples of the plurality of RF signals represented by the sequence of data frames comprising the first data stream; and

a digital to analog converter for converting the regenerated sequence of samples at the sample clock rate into an analog signal comprising a regenerated version of the plurality of RF signals superimposed on each other.

46. The receiver of claim 45, further including a cable modem termination system (CMTS) coupled to the digital to analog converter for receiving the analog signal and reconstructing therefrom digital messages encoded within each of the plurality of RF signals.

47. An optical signal receiver comprising:

a signal receiver for receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including first and second data streams, the first data stream comprising a first sequence of first data frames, each first data frame representing a sequence of samples of a first RF signal, the second data stream comprising a second sequence of second data frames, each second data frame representing a sequence of samples of a second RF signal;

a first memory device configured to store the first data stream;

a second memory device configured to store the second data stream;

a demultiplexor for receiving the digital data stream, detecting boundaries of the first data frames in the first data stream and of the second data frames in the second data stream

and storing the first data frames in the first memory device and the second data frames in the second memory device;

a clock generator for generating a local sample clock having an associated sample clock rate;

circuitry for simultaneously reading data from the first and second memory devices at a rate corresponding to the sample clock rate and for summing the data read from the first and second memories so as to generate a summed data stream signal; and

an analog converter for converting the summed data stream into an analog signal comprising regenerated versions of the first and second RF signals superimposed on each other.

48. A method of receiving a digital input signal, comprising:

receiving the digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate;

storing the data stream in a memory device at a rate corresponding to the first clock rate;

generating a second clock having an associated second clock rate, and adjusting the second clock rate in accordance with a clock control signal;

reading data from the memory device at a rate corresponding to the second clock rate;

generating a fullness signal that indicates whether the memory device is more full than a predefined threshold fullness level; and

generating the clock control signal in accordance with the fullness signal.

49. The method of claim 48, wherein the second clock is generated using a voltage controlled crystal oscillator and the clock control signal is a voltage signal.

50. A method of receiving a digital input signal, comprising:

receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including a first data stream having an associated first data rate and a second data stream having an associated second data rate that is different from the first data rate; the first data stream comprising a sequence of data frames, each data frame representing a sequence of samples of an RF signal;

detecting boundaries of the data frames in the first data stream and storing the data frames in a first memory device, and identifying data in the digital data stream comprising the second data stream and storing the second data stream in a second memory device;

generating a local sample clock having an associated sample clock rate;

reading data from the first memory device at a rate corresponding to the sample clock rate so as to regenerate the sequence of samples of the RF signal represented by the sequence of data frames comprising the first data stream; and

converting the regenerated sequence of samples at the sample clock rate into an analog signal comprising a regenerated version of the RF signal.

51. The method of claim 50, including:

generating a fullness signal that indicates whether the first memory device is more full than a predefined threshold fullness level;

generating a clock control signal in accordance with the fullness signal; and

adjusting the sample clock rate in accordance with the clock control signal.

52. The method of claim 50, including reading data from the second memory device and transmitting the data read from the second memory device to a digital data device.

53. The method of claim 52, wherein the digital data device is a data processor.

54. The method of claim 52, wherein the digital data device is coupled to a network router for routing data packets in the second data stream.

55. A method of receiving a digital input signal, comprising:

receiving the digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including first, second and third data streams, the first data stream comprising a first sequence of first data frames, each first data frame representing a sequence of samples of a first RF signal, the second data stream comprising a second sequence of second data frames, each second data frame representing a sequence of samples of a second RF signal;

detecting boundaries of the first data frames in the first data stream and of the second data frames in the second data stream and storing the first data frames in a first memory

device and the second data frames in a second memory device, and identifying data in the digital data stream comprising the third data stream and storing the third data stream in a third memory device;

generating a local sample clock having an associated sample clock rate;

simultaneously reading data from the first and second memory devices at a rate corresponding to the sample clock rate so as to regenerate the sequence of samples of the first RF signal represented by the sequence of first data frames comprising the first data stream and the sequence of samples of the second RF signal represented by the sequence of second data frames comprising the second data stream;

converting the regenerated sequence of samples of the first RF signal at the sample clock rate into an analog signal comprising a regenerated version of the first RF signal; and

converting the regenerated sequence of samples of the second RF signal at the sample clock rate into an analog signal comprising a regenerated version of the second RF signal.

56. The method of claim 55, including reading data from the third memory device and transmitting the data read from the third memory device to a digital data device.

57. A method of receiving a digital input signal, comprising:

receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including a first data stream having an associated first data rate and a second data stream having an associated second data rate that is different from the first data rate; the first data stream comprising a sequence of data frames, each data frame representing a sequence of summed samples of a plurality of RF signals, each summed sample comprising a mathematical sum of samples of a plurality of distinct RF signals;

detecting boundaries of the data frames in the first data stream and storing the data frames in a first memory device, and identifying data in the digital data stream comprising the second data stream and storing the second data stream in a second memory device;

generating a local sample clock having an associated sample clock rate;

reading data from the first memory device at a rate corresponding to the sample clock rate so as to regenerate the sequence of summed samples of the plurality of RF signals represented by the sequence of data frames comprising the first data stream; and

converting the regenerated sequence of samples at the sample clock rate into an analog signal comprising a regenerated version of the plurality of RF signals superimposed on each other.

58. The method of claim 57, further including processing the analog signal with a cable modem termination system (CMTS) so as to reconstruct therefrom digital messages encoded within each of the plurality of RF signals.

59. A method of receiving a digital input signal, comprising:

receiving an digital input signal and recovering therefrom a digital data stream and an associated first clock having an associated first clock rate, the digital data stream including first and second data streams, the first data stream comprising a first sequence of first data frames, each first data frame representing a sequence of samples of a first RF signal, the second data stream comprising a second sequence of second data frames, each second data frame representing a sequence of samples of a second RF signal;

detecting boundaries of the first data frames in the first data stream and of the second data frames in the second data stream and storing the first data frames in the first memory device and the second data frames in the second memory device;

generating a local sample clock having an associated sample clock rate;

simultaneously reading data from the first and second memory devices at a rate corresponding to the sample clock rate and summing the data read from the first and second memories so as to generate a summed data stream signal; and

converting the summed data stream into an analog signal comprising regenerated versions of the first and second RF signals superimposed on each other.